REMARKS

Claims 1 - 18 have been canceled and new claims 19 - 45 have been added. Claims 19 - 45 are now pending in this application.

The specification is amended to add a cross reference to the prior application and to correct minor typographical errors. No new matter is added by way of these amendments.

The application filing fee as calculated on the application transmittal sheet reflects the amendments to the claims described above.

The Applicant respectfully requests that the preliminary amendment described herein be entered into the record prior to examination and consideration of the above-identified application.

Respectfully submitted,

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This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to the Commissioner for Patents, Box Patent Application, Washington, D.C. 20231.

Docket No. 00303.221US5 Micron Ref. No. 94-0108.04
WD #

Clean Version of the Amended Specification Paragraphs

ON-CHIP SUBSTRATE REGULATOR TEST MODE
Applicant: Gary R. Gilliam
Serial No.: Unknown

Please replace the paragraph beginning on page 4, line 19, with the following:

For example, in Figure 1, the non-test condition of EN1 may be at a logical low so that the MOSFET M3 is in the diode chain because the MOSFET M4 is off. The non-test condition of EN2 may be at a logical high so that the MOSFET M5 is essentially shorted out of the diode chain because the MOSFET M6 is on. Therefore, the voltage level of the substrate at node Vbb, under non-test conditions, is substantially equivalent to the supply voltage level Vcc, less the voltage dropped by the three MOSFETs M1, M2 and M3. Under test conditions, the voltage level at node Vbb can be made more positive by raising the control signal EN1 to a logical high. Such an enabling of the control signal EN1 turns on the MOSFET M4 which essentially shorts the channel of the MOSFET M3 thereby removing the MOSFET M3 from the diode chain, so that the voltage level at Vbb is substantially equivalent to the supply voltage level Vcc, less the voltage dropped by only the MOSFETs M1 and M2. The normal substrate voltage level at Vbb can then be restored by returning the control voltage EN1 to a logical low.

Please replace the paragraph beginning on page 6, line 16, with the following:

The addition of the MOSFETs M7, M8, M9 and M10 to the circuit increases the adjustability of the substrate voltage level Vbb, beyond that of the circuit shown in Figure 1. For example, the non-test condition for the control signals EN1 and EN2 may be a logical low so that the MOSFETs M3 and M5 are in the diode chain. The non-test condition for the control signals EN3 and EN4 may be a logical high so that the MOSFETs M7 and M8 are essentially shorted out of the diode chain. Under test conditions, the substrate voltage level Vbb may be made more positive by raising the control signal EN1 to a logical high and essentially shorting the MOSFET M3 out of the diode chain. The substrate voltage level Vbb can then be made even more positive

by raising the control signal EN2 to a logical high and essentially shorting the MOSFET M5 out of the diode chain, as well. The normal substrate voltage level at Vbb can then be restored by returning the control signals EN1 And EN2 to a logical low. The substrate voltage level Vbb, can be made more negative from its non-test condition by lowering the control signal EN3 to a logical low and thereby adding the MOSFET M7 to the diode chain. The substrate voltage level Vbb, can then be made even more negative by lowering the control signal EN4 to a logical low and adding the MOSFET M9 to the diode chain.